Frequency Synthetic Unit FS702

Description

1. General

FS702 is a digital frequency synthetic unit constructed according to the analytic principle as a phase locked loop. It replaces the common crystal oscillator unit and provides a maximum of 100 channel frequencies with 25kHz skips for the transmitter as well as the receiver. In addition it works as modulator on the transmitter side.

2. Block diagram

3. Mode of operation

As shown in the block diagram, the unit consists of 7 sub-units 1) a reference oscillator. 2) a phase detector with filter. 3) a voltage controlled oscillator with modulation amplifier. 4) a two-divider with pre-amplifier. 5) a programable frequency divider and finally 6) and 7) output amplifiers.

The output frequency is generated in the voltage controlled oscillator. From here the signal is fed to the two output amplifiers plus via a third amplifier, a two-divider and a programable frequency divider to the phase detector, where it is compared with the refrerence frequency of 12.5kHz. The output voltage of the phase detector is filtered and fed to the varactor diode of the VCO, which makes up the capacity in the oscillating circuit of the oscillator. The excitation will affect the capacity of the varactor diode and with it the resonance frequency

38-424

of the oscillating circuit in such a way that the output frequency from the programable frequency divider will become equal to the reference frequency 12,5kHz, and in addition, the phase between the 2 frequencies will become zero, thus that the output frequency of the VCO becomes exactly 12,5kHz x N x 2. It is also dependent of the dividing proportion N, which is adjusted by the BCD code signals from the channel selector. When modifying N to N + 1, the output frequency will be modified f = 12,5kHz x (N + 1) z 2 - 12,5kHz x N z 2 = 25kHz.

4. Individual examination of the units

4.1 The reference oscillator consists of a 3,2 MHz crystal oscillator and a fixed frequency divider. The oscillator is a colpitt coupled fundamental tone oscillator, which swings on the parallel resonance of the crystal. The collector load of the transistor consists of a 15uH throttle parallel with 150pF. This will give a certain filtering of the output frequency, so that the 2nd. harmonic cannot interfer. The output signal is fed via a RC network to the frequency divider. The RC-network is essential in order to obtain correct level for logic "0" ($V \leq 0.8$ V d.c.). The frequency consists of 2 binary 16 bits dividers. The dividing proportion is 16 x 16 - 256 and the output frequency will be 3,2MHz: 256 = 12,5kHz. The signal is a symmetrical square voltage.

4.2 The phase detector consists of the detector MC4344 itself with built-in active filter plus a LC filter. We are talking about a digital circuit, which output voltage is controlled by a shift between high and low level on the 2 inputs. The unit operates both as frequency and phase detector. The same circuit has a built-in amplifier, which in connection with the external components makes up an active filter. The filter constants determine, together with the amplificatic of the phase detector and the VCO, the primary loop constant, resonance frequency ω_n and the attenuation ζ and with it the quality of the noise close to the output frequency plus the transient time. Since the active filter cannot alone attenuate the reference frequency 12.5kHz sufficiently, a LC filter of 80 mH 10uF has been added. It has so high a limiting frequency $>5 \times \omega_n$ that the quality of the loop cannot be affected.

FS702
38.927

4.3 The voltage controlled oscillator consists of the oscillator itself plus a pre-emphatic and compensation sircuit for the modulation. The oscillator circuit is composed of a varactor capacitor plus a coil in the first transistor collector. The signal is taken across the collector of the second transistor, while the negative feedback is made across the emitter of the second transistor back to the emitter of the first transistor. We are talking about a kind of Buttler oscillator. The varactor diode consists of 2 diodes with the cathodes coupled together in order to out-compensate the rectified RF voltage. In return one will get half the modifi capacity. The 2 diodes are dc decoupled to chassis by means of a throttle. The coupling between the 2 transistors consists of a little capacitor of 4,7pF in order to lead the circuit as little as possible. It is important to achieve a high circuit Q with regards to the qualities of the oscillator noise. The excitation is fed to the 2 diodes via 4,7K ohms. The modulation is applied parallel to the excitation. We are talking about frequency modulation. However phase modulation is desired. This is made by inserting a RC-network, which gives 6 dB/octave (21,R26). Since the characteristic of the control diode is curved, one will not get the same modulation sensitivity across the band. If the limiter is adjusted to a frequency swing of ±5kHz for f = 15 MHz, fm = 1000 Hz, the frequency swing will perhaps only be ±2 kHz for f = 17,5 MHz. This is of course unacceptable. It is for this reason that a transistor amplifier has been added, which will counteract the vurved characteristic of the diode. The circuit operates as follows:

The base distortion of the transistor is partly obtained from a high ohmed voltage divider and partly from the excitation from the varactor diode, which is fed back via 2 x 10 K ohms and decoupling capacitor. The decoupling is essential, otherwise the transistor would be negative feedback. The amplification of the transistor is now partly controlled by the varactor excitation. The excitation is low at low frequencies, and the amplification of the transistor is therefore also low. The excitation will increase at high frequencies and with it the amplification. Since the modulation sensitivity is high for low frequencies and low for high frequencies, one can adjust the amplification of the transistor in order to get the same sensitivity across the whole band. The adjustment in made by letting the

fixed base distortion form a larger or a lesser part of the total distortion (28).

The output voltage of the transistor is fed via a decoupling (C 27) to the varactor diode. The cut-off frequency of the decoupling should be set so high that it cannot affect the modulation. The purpose of the filter is to block the low-frequency noise of the transistor, since the varactor diode is very sensitive.

4.4 Two-divider and pre-amplifier.

Since the programable frequency divider cannot work with frequencies which are higher than approx. 12 MHz, it is necessary to couple a 2-divider in front. The reference frequency should at the same time be reduced to half the channel space, therefore 12,5kHz. The 2-divider should therefore work with frequencies up to 17,5MHz (highest output frequency). The pre-amplifier is necessary in order to obtain sufficiently high trigger level and in order to insulate the 2-divider from the output. Using a tuned amplifier for better insulation would have been an advantage, but this was not possible by the space available. It is for this reason that the output voltage contains a weak spurious on half the frequency $\sim$ 8 MHz. The amplifier is coupled to the 2-divider with a RC-network in order to obtain correct DC level for logic "0" ($V \leq 0,8V$). The throttle in the bottom of the resistor will prevent strong attenuation by the signal. SN54H72 is used as 2-divider, since the standard circuit SN5472 cannot work with 17,5MHz with certainty. It is possible to increase the frequency to 24MHz with SN54H72, therefore output frequency 12 MHz, which is the max. working frequency of the N-divider.

4.5 The programable frequency divider consists of 3-decade counters SN64160 and a gate circuit SN6400.

The mode of operation is as follows:

The counter No. 1 has both enablers on "1" and will count at each clock impulse. The counter NC. II (tens) will only count when getting "carry" signal from the conter 1. The counter No. III (a hundred) will only count when getting a "carry" signal from both 1 and 2. The gate circuit detects position 998 and will at the next clock impulse give output signal, which is simultaneously fed to the load inputs of all 3 counters. This will insert a number in the counters depending of the voltages on the 3 x 4 control inputs. The number "loaded" is

the complement of 9 of the dividing proportion expressed in BCD.

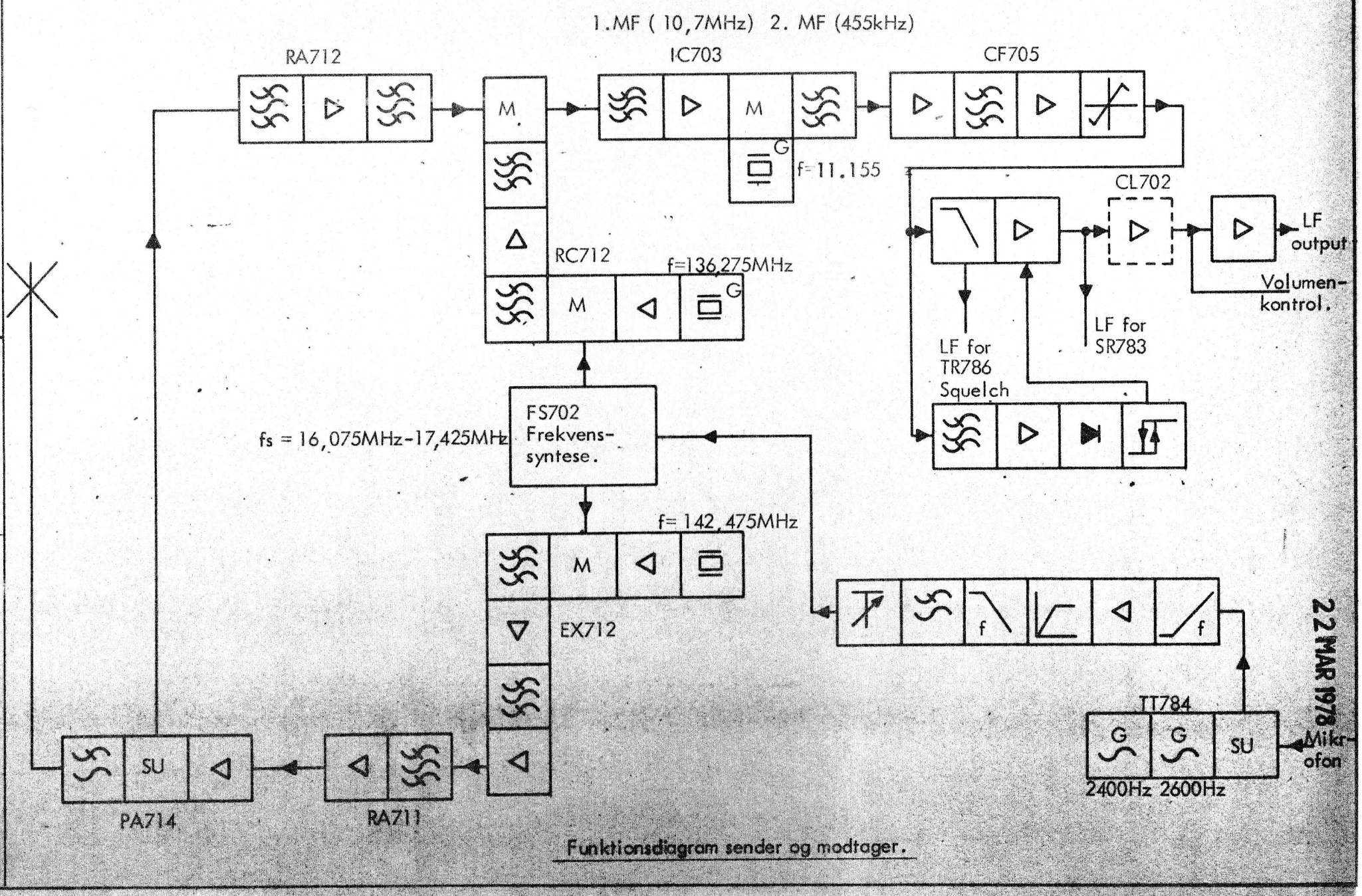
If for example the dividing proportion 345 is desired, the number 654 should be inserted in the counter.

The counter sequence will therefore be as follows:

This means that the counter is dividing with 345. Since the load signal exist before the clock impulse No. 346, one will not loose any impulses, not even at high frequencies. Max. counter frequency is approx. 12MHz.

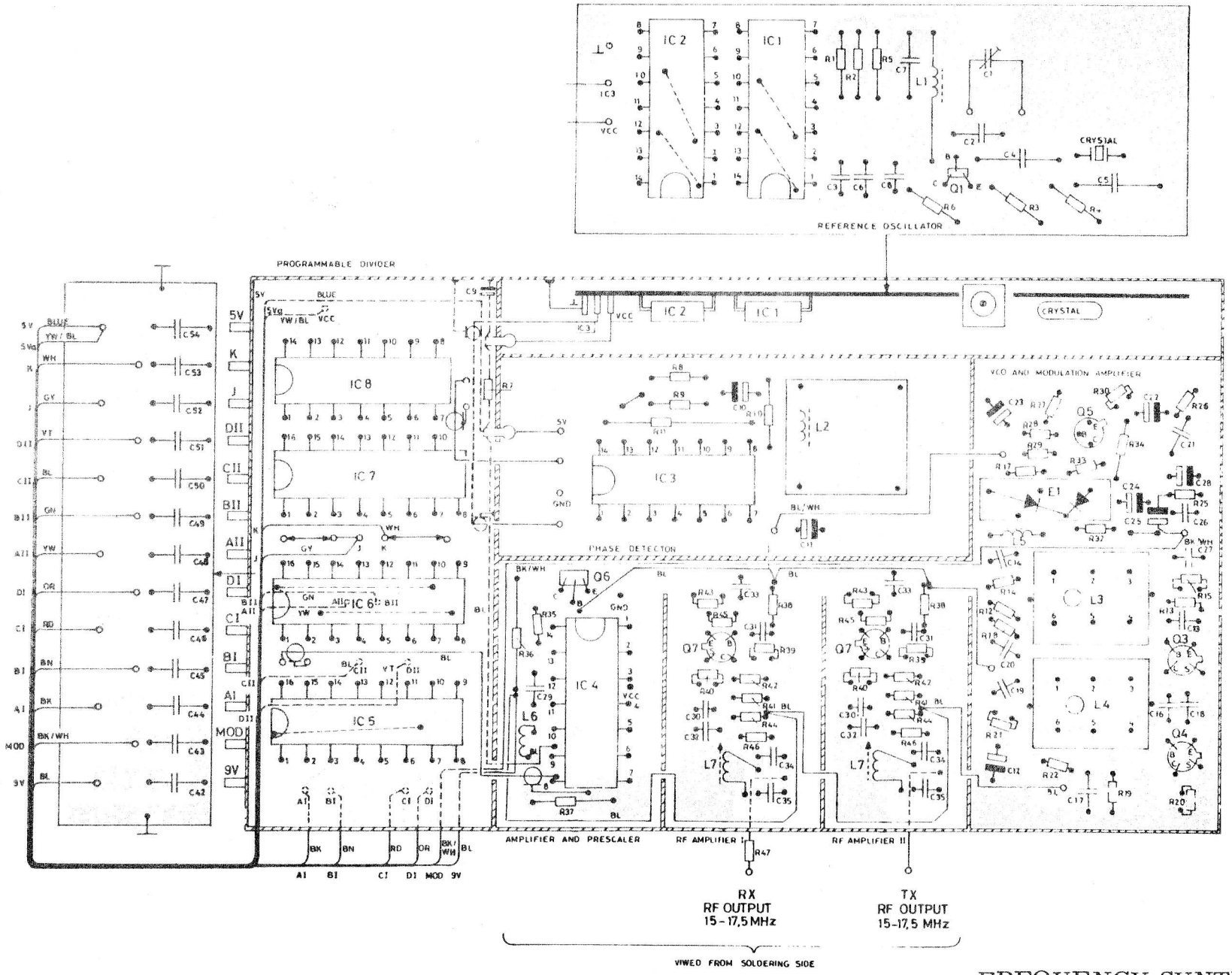
If it is desired that the adjusted control signal should corresponds to the dividing proportion, it would have to be converted into the complement of 9 in BCD.

4.6 The output amplifiers are tuned amplifiers with BSX89. The output circuit is attenuated with 1K ohm in order to obtain 3 MHz bandwidth. The bandwidth lies 100 ohms in series with input in order to separate the 2 outputs from each other, and in order not to load the VCO too much. There is a none decoupled emitter resister of 56 ohms, which will improve the attenuation of the harmonics substantially. This is of importance, since filter between the output of FS702 and the 2 mixer inputs in RC and EX respectively does not exist.



Funktionsdiagram sender og modtager.

22 MAR 1978



FREQUENCY SYNTESIZER
FREKVENSSYNTESEENHED

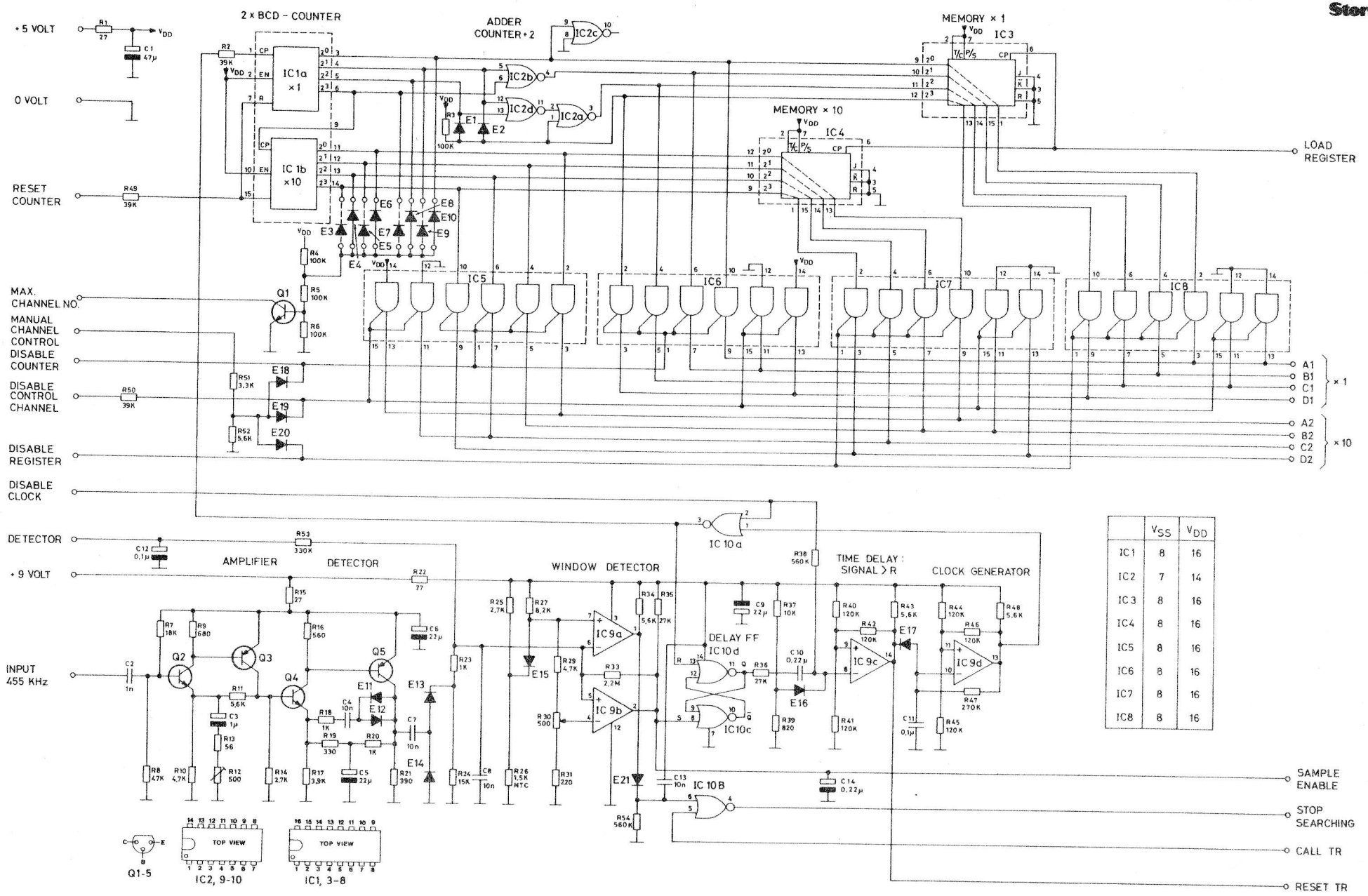
FS702

402.550

Storno

25 MAY 1978

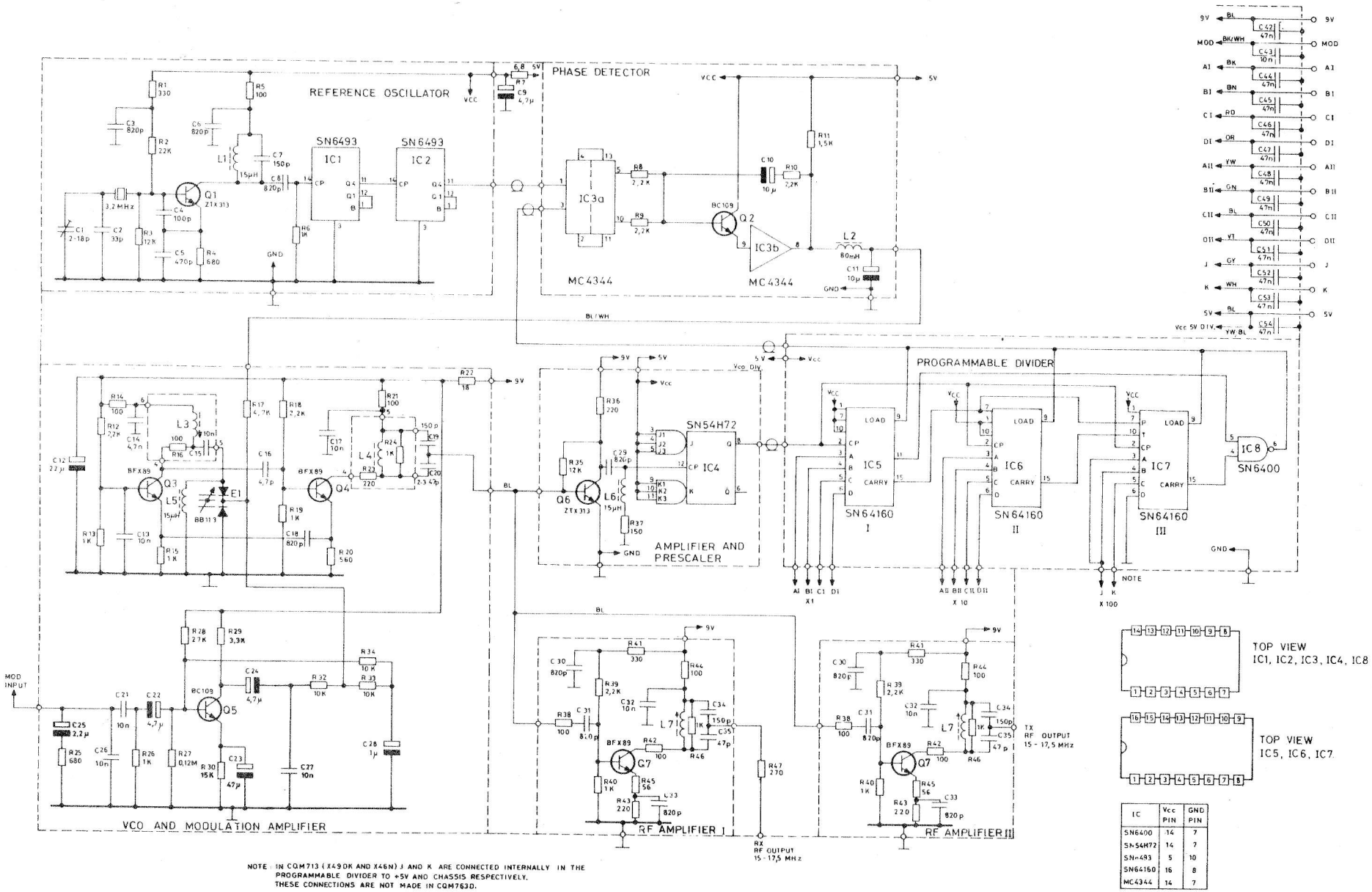
Storno



	V_{SS}	V_{DD}
IC1	8	16
IC2	7	14
IC3	8	16
IC4	8	16
IC5	8	16
IC6	8	16
IC7	8	16
IC8	8	16

FREQUENCY CONTROL UNIT FC705

D 402.383/2



IC	Vcc PIN	GND PIN
SN6400	14	7
SN54H72	14	7
SN6493	5	10
SN64160	16	8
MC4344	14	7

NOTE : IN CQM713 (X490K AND X46N) J AND K ARE CONNECTED INTERNALLY IN THE PROGRAMMABLE DIVIDER TO +5V AND CHASSIS RESPECTIVELY. THESE CONNECTIONS ARE NOT MADE IN CQM7630.

I CQM713D (X490K OG X46N) ER J OG K STRAPPET TIL H.H.V. 5V OG STEL INTERNT I DEN PROGRAMMERBARE DELER.
I CQM7630 ER OVENNÆVNTE STRAPNING IKKE INDFØRT.

FREQUENCY SYNTESIZER
FREKVENSSYNTESEENHED FS702

D 402.406

REVISED

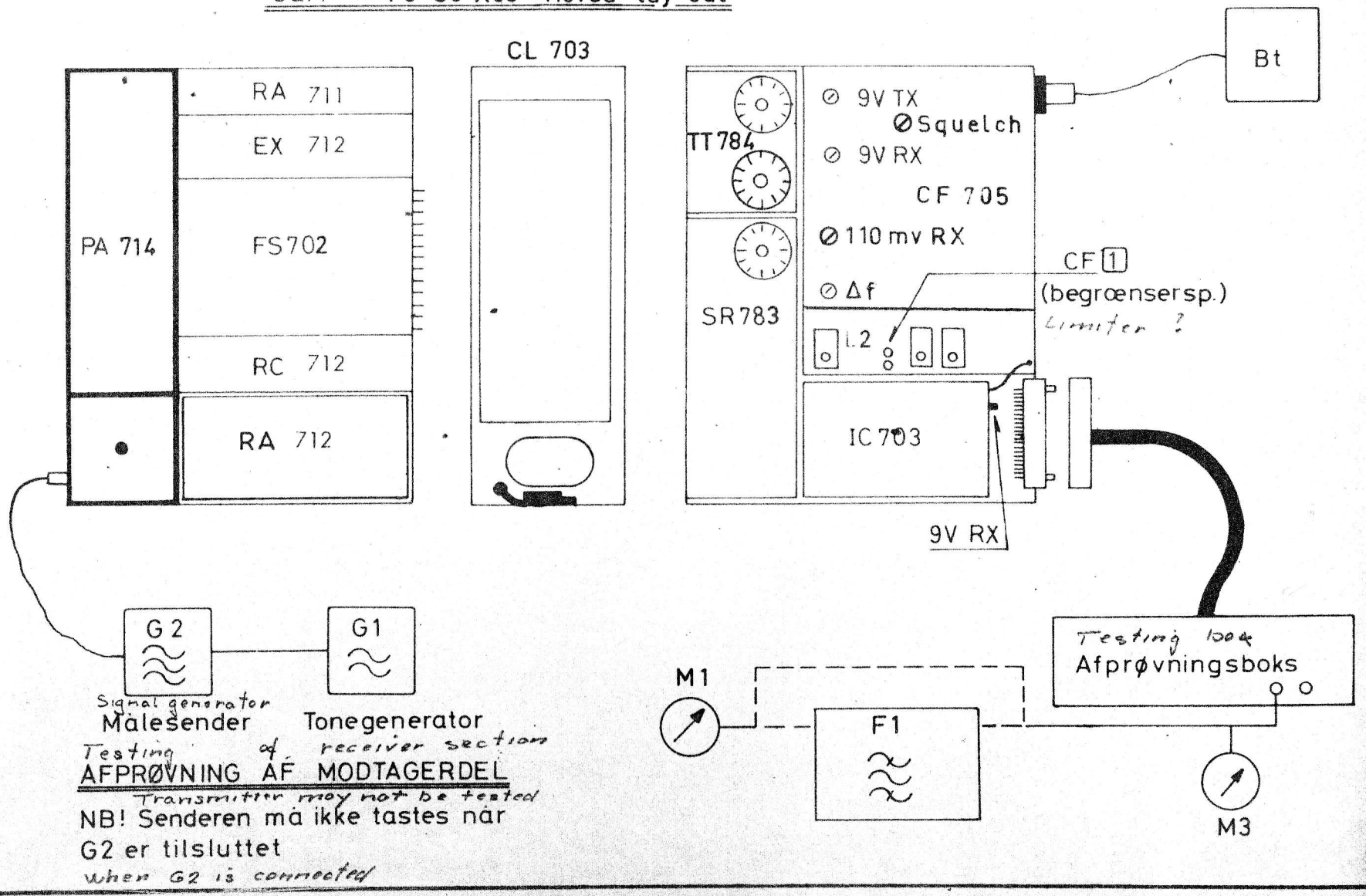
ONH-5230 29-10-76

Storno

Afprøvningsforskrift, 38.716
CQM713 P3 C6X55
4 af 30

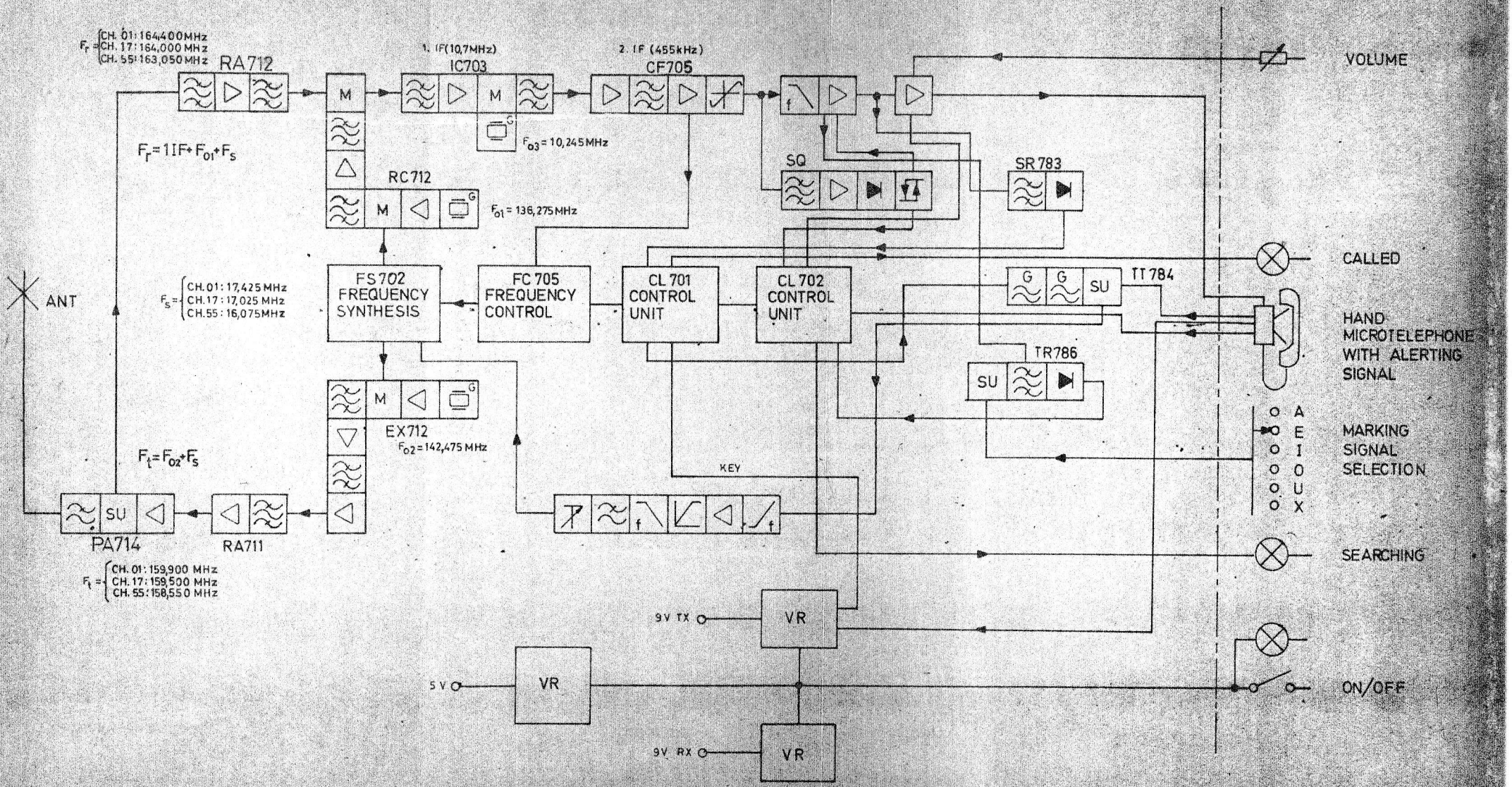
Main

CQM 713 P3 C6 X55 Hoved lay-out



17 NOV 1976

55 CHANNEL MOBILE EQUIPMENT FOR RADIOPHONE SYSTEM 3



27.1.76 BØ	KJ BØ	FUNCTION DIAGRAM CQM713 P3 Spec C6 X55	25.6.75
	Storno		D402.136

Ændret: 29.12.75. KSN
20.5.76. Bø